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Fatigue Life Estimation of TQLMP Integrated Circuit Packages Using Coupled Field Finite Element Analysis and Acoustic Microscopy

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Thermal- structural analysis,
Fatigue life,
Coffin-Manson Equations.

Abstract

This investigation presents a general methodology of failure analysis and fatigue life prediction of a selected electronic package. The quad packages are relatively new and have high design complexities. Thin Quad Leadless Moulded Package (TQLMP) is the type of chip considered here for analysis. In this investigation complete 3D modelling of production level TQLMP ICs is designed using SOLIDWORKS software. It is analysed for electro – thermal- mechanical properties and fatigue life using ANSYS finite element modelling software. Coupled field analysis is the type considered here for solution. Output from electro-thermal analysis is considered as input for thermal-structural analysis in the coupled-field analysis. Thermal stresses and plastic strains which arise due to the joule heating developed within the packaging are considered here for the fatigue evaluation of the package. Displacements, tensile and compressive stresses and shear stresses rising from deformation are evaluated. Fatigue life curve is finally plotted using the Coffin-Mansons equation.

The work had been presented *at an* international conference ***Fatigue Durability India 2015****, 28-30th May 2015, JN TATA AUDITORIUM, Indian Institute of Science, Bangalore.*

Introduction

The very basic parts of any electronic device are the chips. Microelectronics typically refers to to those micro devices, such as integrated circuits which are the very basis of all the electronic products. They are fabricated in sub-micron dimensions. “Systems” refers to all electronic products. “Packaging” is a connecting element between the ICs and the other components into a system level board to form electronic products. The main role of a package in the electronic system is to shut out the environmental influences, enable electrical connectivity, dissipate heat and improve handling and assembly and also to increase the reliability of the electronic product.[1]

In the present study, the complete models of the 24L ,36 L and 64 LTQLMP ICs are designed in Solid Works and analysed for electro-thermal-mechanical properties using the a finite element modelling software ANSYS. As the IC packages experience joule heating during their operation due to the application of the voltage and current, they cause the thermal stresses to be induced in the package. These thermal stresses cause warping, bending and other type of deflections and mechanical stresses develop in the package that is fixed to a PCB.

Thermo mechanical failures are caused by stresses and strains generated within an electronic package due to thermal loading from the environment or internal heating in service operation. Due to the mismatch in the coefficient of thermal expansion (CTE) among different materials, due to thermal gradients in the system, and due to geometric constraints, thermally-induced stresses and strains are generated in various parts of a system. Among the various thermo-mechanical failure mechanisms fatigue, cracks, brittle fracture, creep, interfacial delamination, and plastic deformation are the most predominant ones.

Due to the CTE mismatch of laminated materials, under the cyclic thermal loading, the stress and strain development in the free edge of the solder layer will be the main concern in the design and fabrication of semiconductor device packaging. Using finite element analysis and damage mechanics for a constitutive model it is possible to predict the number of cycles to failure for solder layers [3]. An accurate estimate of thermal stresses in multi layered microelectronics structures along the bonded interfaces is crucial for design and prediction of delamination-related failures. Compared with a numerical method, analytical closed-form solution can offer a more rapid solution to obtain the stresses at the interfaces. The theory presented treats each layer as a beam-type plate with orthotropic material properties. Thermal stresses that occur due to CTE mismatch of the adhesively joined materials, during manufacturing, machining, and field use can result in delamination type of failures [4].

The fatigue life of metals which undergo cyclic mechanical stresses can be understood only with the help of strains [5]. In this investigation, the plastic strains developed during the joule heating process of the TQLMP ICs are used to predict the fatigue life of the copper lead frame- encapsulant interface which is the weakest area in the ICs as evinced through the Scanning Acoustic Microscopy (SAM) images of preconditioned samples. The Coffin-Manson relationship is used here to find out the fatigue behaviour of the ICs.

Static electro thermal analysis

A coupled-filed analysis is a combination of analyses from different engineering disciplines (physics field) that interact to solve a global engineering problem. Hence, we often refer to a

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coupled-filed analysis as a multiphysics analysis in the ANSYS software.

Types of coupled-field analysis

Sequential:

The *sequential method* involves two or more sequential analyses, each belonging to a different field. Two fields can be coupled by applying *results* from the first analysis as *loads* for the second analysis. An example of this is a sequential thermal-stress analysis where nodal temperatures from the thermal analysis are applied as "body force" loads in the subsequent stress analysis.

Direct method:

The *direct method* usually involves just one analysis that uses a *coupled-field element type* containing all necessary degrees of freedom. Coupling is handled by calculating element matrices or element load vectors that contain all necessary terms. Direct method usually involves just one analysis that uses a coupled field element type containing all necessary degrees of freedom.

Modeling

Totally three packages were taken for in this project, viz. the 4x4mm 24L, 5x6mm 36L and the 9x9mm 64L TQLMP (Thin Quad Leadless Moulded Package). Firstly, the 2D and the 3D models of the packages were created according to prescribed dimensions. In the next step, the coupled field thermo-structural analysis of 3D model was carried out for determining various stresses and strains induced in the package.

Modelling of the 4x4mm 24L, 5x6mm 36L and the 9x9mm 64L package was done with the help of solidworks 2014 software. The IC package consists of three different layers built one on one such as the lead frame, adhesive epoxy , the die and the gold wire bonding. Finally the IC mould package is encapsulated over them. Initially the sketching plane and reference plane are selected. Then the parts are produced one by one by using the following feature operations, such as, Lead frame – Extrude, fillet and linear pattern Adhesive Epoxy, Silicon die – Sketch & Extrude Gold wire – Sweep & extrude cut and Encapsulation – Sketch & Extrude. After creating individual parts it can be assembled one by one by using mating, bonding and gluing options. Reference planes and faces are selected for the mating operation. Lead frame followed by adhesive epoxy, Silicon die, Gold wire and finally the encapsulation is the sequence followed.

4x4mm 24 LTQLM package

Initially the lead frame with thickness of 0.2mm having 24 leads was constructed with each side having 6 leads. Lead frame dimensions are 2x2.8x.2 mm. Leads were circular at the edge with a radius of 0.25mm. The adhesive epoxies with dimensions of 2.22x2.06x0.25mm and the silicon die with dimensions of 2.22x2.06x0.2 mm were modelled. There are 24 leads and the gold wire is bonded on to the silicon die. Diameter of the gold wire is 0.025 mm (around 25 microns).Length of each lead is 0.35mm and distance between centres of each lead is 0.5mm. The final encapsulant dimensions are 4x4x1mm.

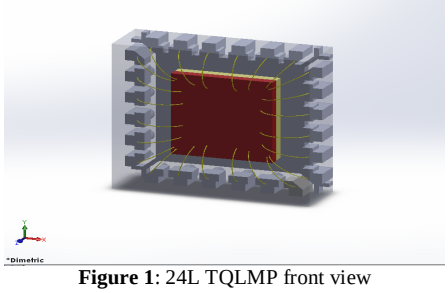

Figure 1: 24L TQLMP front view

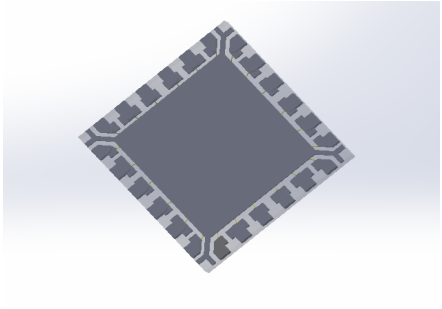

Figure 2: 24 L TQLMP back view

Similarly the 36 L and 64 L TQLMP models were created using the dimensions provided by the production drawings. Otherwise, the general architecture was similar. The numbers 24, 36 and 64 refer to the pins provided at the bottom of the IC packages.

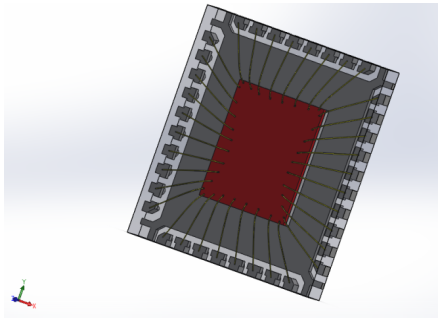

Figure 3: 36 L TQLMP with encapsulant

The 9x9mm 64 L TQLM package

It is similar to the above type of packages except in dimensions. 4.92 x 4.92 x 0.25mm is the size of the pad and 7x7x0.2 mm is the lead frame size. Because of design and analytical complexities a simplified model is considered here which is scaled according to dimensions.

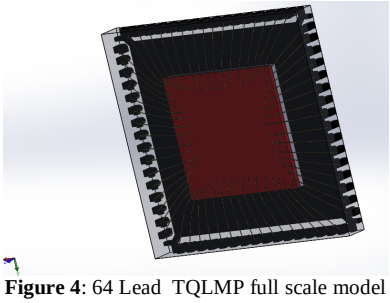

Figure 4: 64 Lead TQLMP full scale model

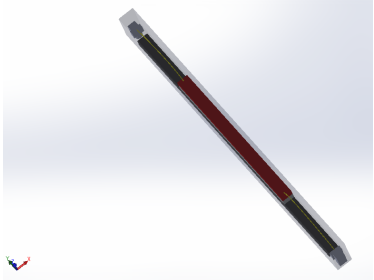

Figure 5: Simplified and sliced model of 64Lead TQLMP

ELECTRO THERMAL ANALYSIS OF 24L, 36L AND 64 L TQLMPs

In this analysis we consider the electrical and thermal field. In the electrical field the voltage difference is input as load and as an output we get the temperature distribution and electric potential. From this we get the result as the temperature gradient in the packaging. Analysis was carried out using a condition of the reference temperature at 24^o C out side the package under conditions of forced convection. Before performing the analysis we must obtain the proper material property for the concerned IC package. In this project, the following materials were used in manufacturing:

Lead frame – Copper, Silicon die – Doped silicon, Adhesive Epoxy- Silver epoxy, Encapsulant - Carbon black, fused silica particles filled with epoxy and phenolic resin.

Table 1 : Bill of materials and their properties

Materials	Young's modulus (N/mm^2)	Poisson's ratio	CTE (/^{0}C)	Thermal conductivity (W/mm^{0}C)	Electrical resistivity (Ω-mm)
Copper	110.31e3	0.22	16.50e-6	401e-3	1.673e-5
Silver epoxy	11.5e3	0.35	30e-6	546e-3	8e-4
Silicon	200e3	0.25	2.60e-6	130e-3	1
Gold	82.737e3	0.44	14.20e-6	317e-3	2.350e-5
Filled epoxy	26e3	0.25	7e-6	0.0012	10e5

Procedure:

The model was imported from solidworks in the IGES format. The material property for the concerned part as per the table-1 was assigned. The volumes were meshed using the mesh option. A voltage difference to the given leads for 24L (5 volts in lead 1 and 0 volts in lead 8),for 36L (1.8 volts in lead 1, 5, 10, 23, 28and 0 volts other leads) and for simplified 64L(1.8volts on one and 0 on other lead) was applied. An outer surface temperature of 24^o C on the top side of encapsulant was considered. Convective heat transfer coefficient (forced convection) of 200 W/m^2 at a reference temperature of 24^o C was also added. The analysis Results are given below.

24L TQLMP Electro thermal output

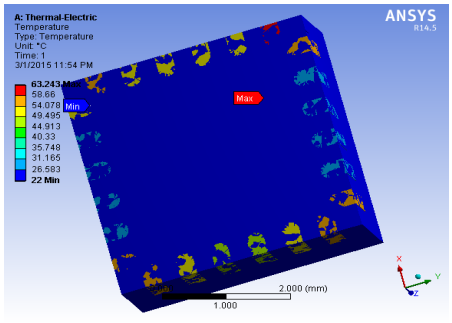

Figure 6: 24L TQLMP temperature distribution with encapsulant

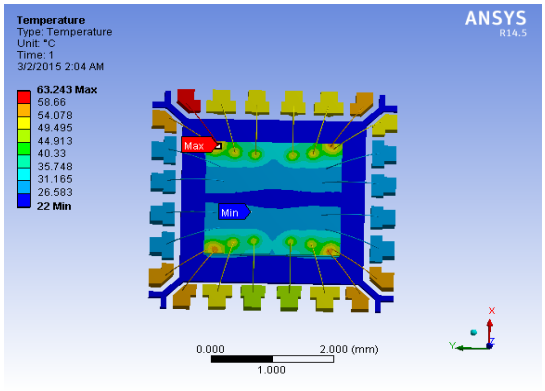

Figure 7: 24L TQLMP temperature distribution (with out encapsulant)

36L TQLMP Electro thermal Output:

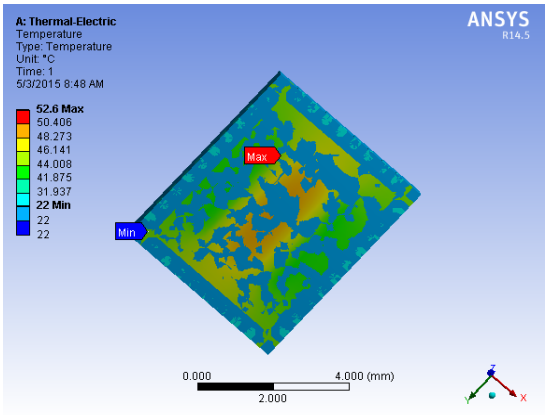

Figure 8: 36L TQLMP temperature distribution with encapsulation

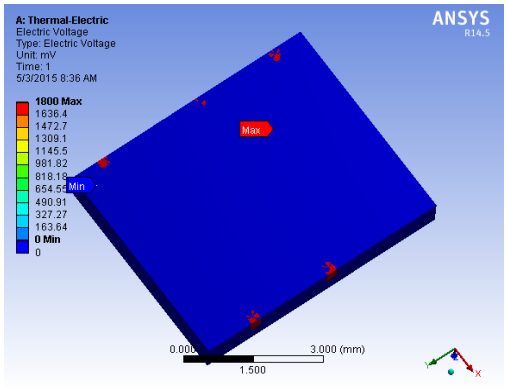

Figure 9: Voltage plot for 36 TQLMP with encapsulation

64 L TQLMP electrothermal output

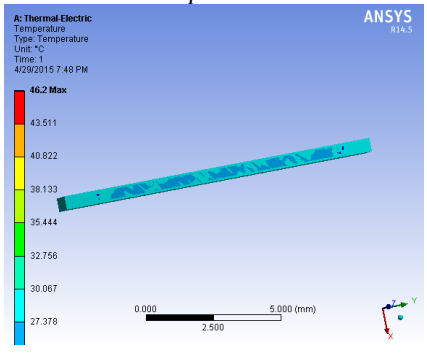

Figure 10: Temperatur plot for Sliced 64L TQLMP

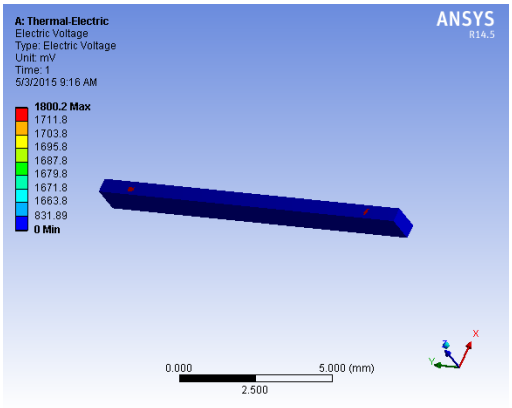

Figure 11: Potential difference applied for 64 L TQLMP

THERMO MECHANICAL ANALYIS AND FATIGUE ESTIMATION OF 24L, 36L & 64L

In this coupled field analysis we consider the thermal and structural field. In the thermal field, with temperature obtained during joule heating as the input load, we obtain the temperature gradient as output . From this result and with the properties like CTE as input in the structural field , we get the output as deformation, shear stress, von mises stress etc. The plastic strain is calculated from total strain after subtracting the elastic strain. The plastic strain is important in the estimation of the fatigue life through the coffin-Manson relationship.

After completing the electro thermal analysis, the results are transferred to a static thermal-structural analysis. Young's modulus, poisons ratio and coefficient of thermal expansion (CTE) are to be mentioned accordingly to the material specified in table - 1 to solve the static structural results .Results are shown below.

24L TQLMP structural output

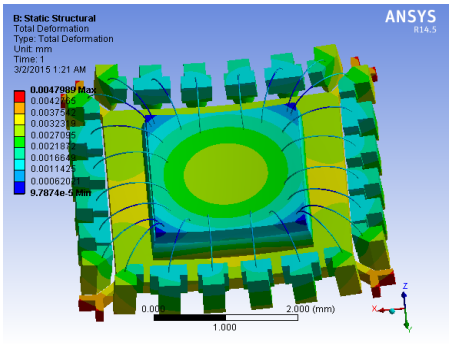

Figure 12: Total Deformation plot

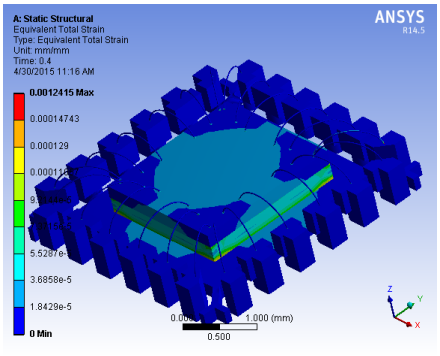

Figure 13: Total equivalent strain plot

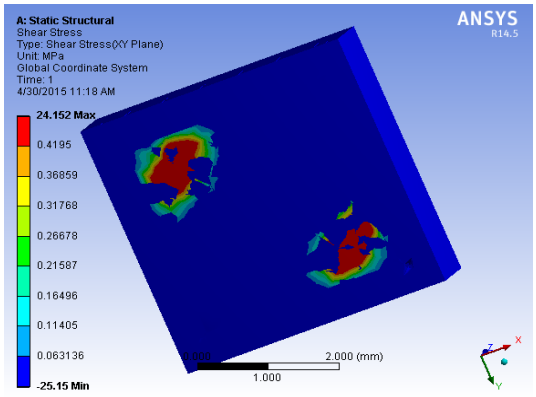

Figure 14: Shear stress (XY) in the encapsulation of the IC

Plastic strain is calculated as = Total strain – elastic strain

From the above figures

Total strain at the copper lead interface ≈ 0.000694465

Shear stress in the pad area between Cu lead frame and encapsulant (XY plane) ≈ 12.28575 MPa

Estimated plastic strain ~ (approx) 0.000307599 to 0.00043

This plastic strain vanishes even at MOT (Maximum Operating Temperature) in the advanced stages of fatigue as at higher cycles the strain becomes more elastic.

36Lead TQLMP structural output:

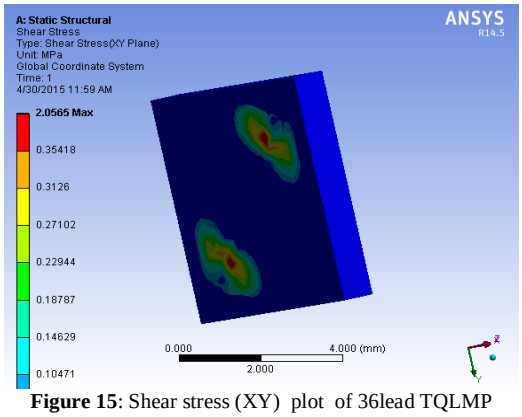

Figure 15: Shear stress (XY) plot of 36lead TQLMP

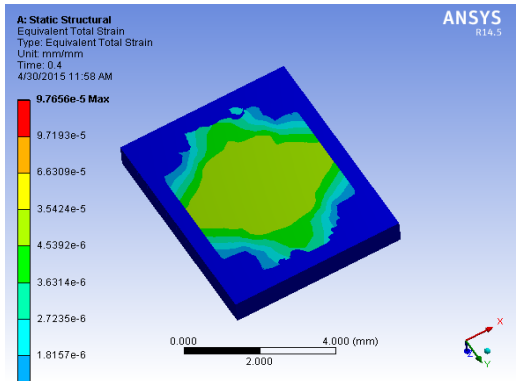

Figure 16: Total equivalent strain (36L)

Total strain ≈ 0.00097656

Shear stress XY plane ≈ 1.504614MPa

Estimated plastic strain ≈ *0.00083977*

Analysis for 9x9mm simplified 64L TQLMP

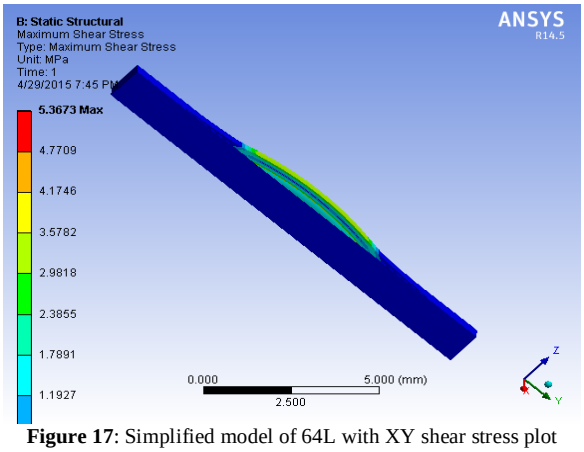

Figure 17: Simplified model of 64L with XY shear stress plot

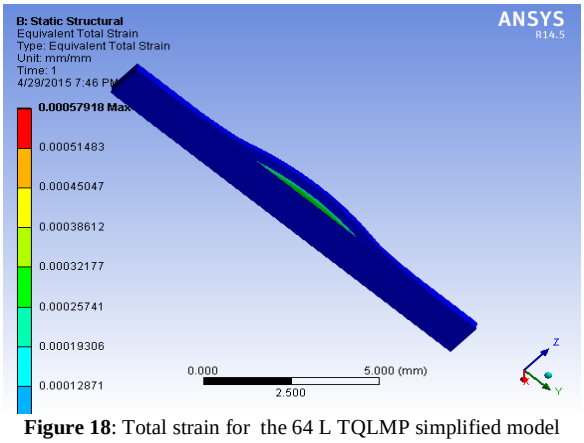

Figure 18: Total strain for the 64 L TQLMP simplified model

Total strain obtained at interface ≈ 0.00028959

Shear stress at Cu- Encapsulant interface ≈ 2.69365 MPa

Plastic strain ≈ 0.0002557

SAM (Scanning acoustic microscopic) results:

Figures 19 and 20 show the SAM images of preconditioned samples that were thermally cycled according to the JEDEC standards. The red areas show delaminations or flaws and it is noticed that the delaminations are usually at the copper lead frame pad area and the encapsulant interface. This area are seen to be the weakest, though its failure does not directly affect the function of the IC. But any moisture ingress causing further damage at the delamination site causes the electrical conductivity of the interface to short the wire bonding that might exist locally which terminates function.

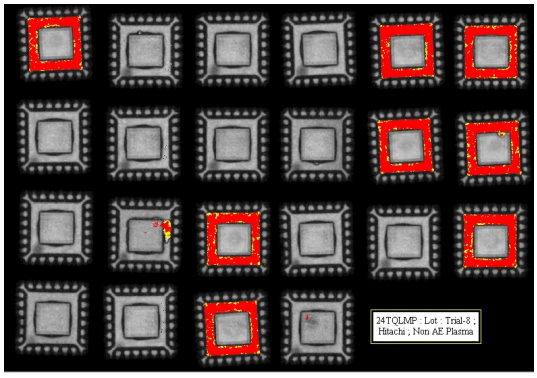

Figure 19: SAM of conditioned 24 TQLMP ICs

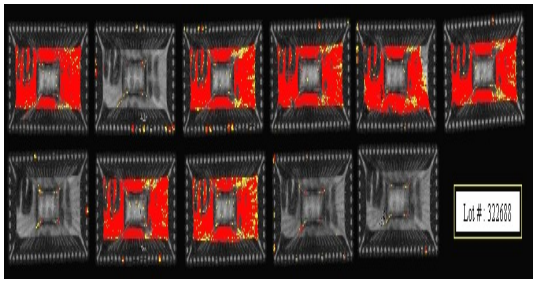

Figure 20: SAM of 36 L TQLMP ICs after conditioning

Results and Discussion

According to Coffin-Manson equations;
$N^{0.5} x\ \delta_p$ = constant
N = Number of cycles; 500 for the Copper lead frame Epoxy interface , from reference [12].

Δ_p = plastic strain , the values of which are taken from the simulation results for the three ICs in this investigation. The plastic strains vary across the width in the pad area. So the values are only about the mean and could influence fatigue by a small factor but with in the scatter of their magnitudes.

Table 2 : Results from the analysis for the three ICs.

	24L	36L	64L
Temperature	63^0C	52.6^0C	46^0C
Deformation	0.00047989mm	0.00095276mm	0.00068463mm
Max Shear stress(XY plane)	24.152 MPa	2.8685 Mpa	5.3673 MPa
Total equivalent strain	0.0012415mm/mm	0.00097656mm/mm	0.00057918mm/mm
Plastic strain	0.0004030mm/mm	0.00083977mm/mm	0.0002557mm/mm

As discussed earlier, the weakest bi material interface at which delaminations occur first is the copper lead frame-encapsulant pad area. Most of the preconditioning experiences have revealed that more than 90 % of the failures occur in the pad area interface. The

following plot , thus, is a Coffin –Manson fatigue graph created to predict the life time of an IC package investigated here.

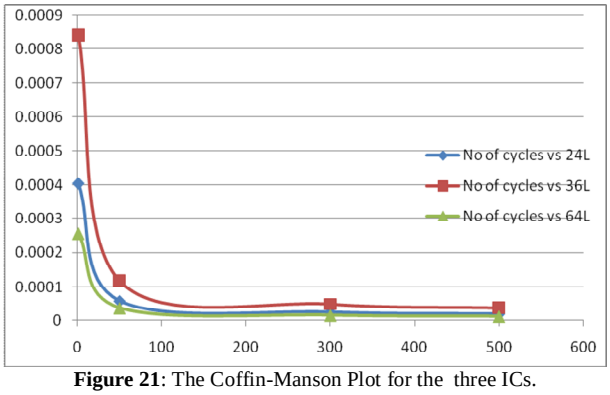

Figure 21: The Coffin-Manson Plot for the three ICs.

Conclusions

Static electro thermal analysis was performed with 24L, 36L and 64L TQLMPs. According to Coffin- Manson equation a graph was plotted between the number of cylces to failure and the plastic strain developed at the interface as a power law. The fatigue lifes of the three TQLMP ICs investigated here, were evaluated using static and fatigue analyses and experimental evidence from SAM.

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